

What is claimed is:

1 1. A processor for reading instructions from a memory
2 according to a program counter, the memory storing
3 instructions in one-byte units, and for executing the read
4 instructions,

5 the program counter including a first program counter
6 and a second program counter,

7 the first program counter indicating a storage
8 position of a processing packet in the memory, the
9 processing packet being composed of an integer number of
10 the one-byte units,

11 the second program counter indicating a position of
12 processing target instruction in the processing packet, the
13 processing target instruction being an operation to be
14 executed by the processor.

1 2. The processor of Claim 1, including a first program
2 counter updating means and a second program counter
3 updating means,

4 the second program counter updating means
5 incrementing a value of the second program counter in
6 accordance with an amount of instructions that were
7 executed in a preceding cycle and sending any carry
8 generated in an incrementing to the first program counter
9 updating means, and

10 the first program counter updating means adding the
11 carry received from the second program counter updating

means to the value of the first program counter.

3. The processor of Claim 2, further including:

program counter relative value extracting means for extracting, when an instruction being executed includes a program counter relative value that is based on an address of a first instruction executed in a present cycle, the program counter relative value; and

calculating means for adding the program counter relative value to the value of the first program counter and the value of the second program counter, and setting an addition result as the value of the first program counter and the value of the second program counter.

4. The processor of Claim 3,

wherein the calculating means includes a first calculating unit and a second calculating unit,
the second calculating unit adding the value of the second program counter and lower bits of the program counter relative value, setting a result of an addition as the value of the second program counter, and sending any carry generated in the addition to the first calculating unit,

the first calculating unit adding the value of the first program counter, upper bits of the program counter relative value, and any carry received from the second calculating unit, and setting a result of an addition as

14 the value of the first program counter.

1 5. The processor of Claim 3,

2 wherein the calculating means includes a first
3 calculating unit and a second calculating unit,

4 the second calculating unit adding the value of the
5 second program counter and lower bits of the program
6 counter relative value without generating a carry, and
7 setting a result of an addition as the value of the second
8 program counter,

9 the first calculating unit adding the value of the
10 first program counter and upper bits of the program counter
11 relative value, and setting a result of an addition as the
12 value of the first program counter.

1 6. The program counter of Claim 3,

2 wherein the calculating means adds the value of the
3 first program counter and upper bits of the program counter
4 relative value, sets a result of an addition as the value
5 of the first program counter, and sets lower bits of the
6 program counter relative value as the value of the second
7 program counter.

1 7. The processor of Claim 3,

2 wherein the calculating means adds the program
3 counter relative value and a value whose upper bits are the
4 value of the first program counter and lower bits are the

5 value of the second program counter, and sets upper bits of
6 a result of an addition as the value of the first program
7 counter and lower bits of the result as the second program
8 counter.

1 8. The processor of Claim 2, further including:

2 program counter relative value extracting means for
3 extracting, when an executed instruction includes a program
4 counter relative value that is based on an address of the
5 executed instruction, the program counter relative value;

6 program counter amending means for amending the value
7 of the first program counter and the value of the second
8 program counter to indicate an address of the executed
9 instruction; and

10 calculating means for adding the program counter
11 relative value, the value of the first program counter, and
12 the value of the second program counter, and setting a
13 result of an addition as the value of the first program
14 counter and the value of the second program counter.

1 9. The processor of Claim 2, further including:

2 program counter relative value calculating
3 instruction decoding means for decoding a program counter
4 relative value calculating instruction that performs an
5 addition using a program counter relative value and one of

6 (a) a value of the program counter stored in a
7 register, and

8 (b) the value of the first program counter and the
9 value of the second program counter;
10 calculating means for performing the addition
11 indicated by the program counter relative value calculating
12 instruction to generate an addition result; and
13 program counter value updating means for storing the
14 addition result in one of
15 (a) the register, and
16 (b) the first program counter and the second program
counter.

10. The processor of Claim 1,

wherein the first program counter indicates a memory
address, the memory address being a storage position in the
memory of a processing packet that is given by bit shifting
the value in the first program counter by $\log_2 n$ bits in a
leftward direction, n being a length of a processing packet
in bytes.

11. The processor of Claim 10, further including
an instruction buffer for temporarily storing
instructions; and

instruction reading means for transferring
instructions with a minimum transfer size of one one-byte
unit from the memory to the instruction buffer, in
accordance with available space in the instruction buffer
but regardless of a size of a processing packet.

1 12. An instruction sequence optimizing apparatus, for
2 generating optimized code from an instruction sequence,
3 comprising:
4 address assigning means for estimating a size of each
5 instruction in the instruction sequence and assigning an
6 address to each instruction, upper bits of each address
7 indicating a memory address at which a processing packet is
8 stored and lower bits of each address indicating a
9 processing target instruction in the processing packet;
10 label detecting means
11 (1) for detecting a label, which should be resolved
12 by an address of a specified instruction, from the
13 instruction sequence, and obtaining the address of
14 the specified instruction, and
15 (2) for detecting a label, which should be resolved
16 by a difference in addresses of two specified
17 instructions, from the instruction sequence, and
18 obtaining the addresses of the two specified
19 instructions;
20 program counter relative value calculating means for
21 calculating, when a label which should be resolved by a
22 difference in addresses of two specified instructions has
23 been detected, a program counter relative value by
24 subtracting an address of one of the two specified
25 instructions from an address of another of the two
26 specified instructions;

27 converting means

28 (1) for converting an instruction that has a label
29 that should be resolved by an address of a
30 specified instruction into an instruction with a
31 size that is based on a size of the address of the
32 specified instruction,

33 (2) for converting an instruction that has a label
34 that should be resolved by a difference in
35 addresses of two specified instructions into an
36 instruction with a size that is based on a size of
37 the program counter relative value calculated from
38 the addresses of the two specified instructions;
39 and

40 optimized code generating means for generating
41 optimized code by converting addresses of instructions in
42 accordance with the sizes of instructions after conversion
43 by the converting means.

1 13. The instruction sequence optimizing apparatus of Claim
2 12,

3 wherein the program counter relative value
4 calculating means includes a lower bit subtracting unit and
5 an upper bit subtracting unit,

6 the lower bit subtracting unit subtracting lower bits
7 of the address of the one of the two specified instructions
8 from lower bits of the address of the other of the two
9 specified instructions, for setting a result of a

subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting unit, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting unit from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

14. The instruction sequence optimizing apparatus of Claim 12,

wherein the program counter relative value calculating means includes a lower bit subtracting unit and an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting unit subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

1 15. The instruction sequence optimizing apparatus of Claim
2 12,

3 wherein the program counter relative value
4 calculating means subtracts upper bits of an address of one
5 of the two specified instructions from upper bits of an
6 address of the other of the two specified instructions,
7 sets a result of a subtraction as upper bits of the program
8 counter relative value, and sets lower bits of the other of
9 the two specified instructions as lower bits of the program
10 counter relative value.

11 16. An assembler that generates relocatable code from an
12 instruction sequence, each address of an instruction in the
13 instruction sequence having upper bits that indicate a
14 memory address at which a processing packet is stored and
15 lower bits that indicate a position of processing target
16 instruction that is included in the processing packet,
17 the assembler comprising:

18 label detecting means for detecting a label in the
19 instruction sequence that should be resolved by a
20 difference in addresses between two specified instructions,
21 and obtaining the addresses of the two specified
22 instructions;

23 program counter relative value calculating means for
24 calculating a program counter relative value by subtracting
25 an address of one of the two specified instructions from an

16 address of another of the two specified instructions; and
17 replacing means for replacing the label with the
18 program counter relative value calculated by the program
19 counter relative value calculating means.

1 17. The assembler of Claim 16,

2 wherein the program counter relative value
3 calculating means includes a lower bit subtracting unit and
4 an upper bit subtracting unit,

5 the lower bit subtracting unit subtracting lower bits
6 of the address of the one of the two specified instructions
7 from lower bits of the address of the other of the two
8 specified instructions, for setting a result of a
9 subtraction as lower bits of the program counter relative
10 value, and sending any carry generated in the subtraction
11 to the upper bit subtracting unit, and

12 the upper bit subtracting unit subtracting upper bits
13 of the address of one of the two specified instructions and
14 any carry received from the lower bit subtracting unit from
15 upper bits of the address of the other of the two specified
16 instructions, and for setting a result of a subtraction as
17 upper bits of the program counter relative value.

1 18. The assembler of Claim 16,

2 wherein the program counter relative value
3 calculating means includes a lower bit subtracting unit and
4 an upper bit subtracting unit,

5 the lower bit subtracting unit subtracting lower bits
6 of the address of one of the two specified instructions
7 from lower bits of the address of the other of the two
8 specified instructions without generating a carry and
9 setting a result of a subtraction as lower bits of the
10 program counter relative value, and

11 the upper bit subtracting unit subtracting upper bits
12 of the address of one of the two specified instructions
13 from upper bits of the address of the other of the two
14 specified instructions, and for setting a result of a
15 subtraction as upper bits of the program counter relative
16 value.

17
18 19. The assembler of Claim 16,

19 wherein the program counter relative value
20 calculating means subtracts upper bits of an address of one
21 of the two specified instructions from upper bits of an
22 address of the other of the two specified instructions,
23 sets a result of a subtraction as upper bits of the program
24 counter relative value, and sets lower bits of the other of
25 the two specified instructions as lower bits of the program
26 counter relative value.

27
28 20. A linker that generates object code by combining
29 relocatable code, each address of an instruction in the
30 relocatable code having upper bits that indicate a memory
31 address at which a processing packet is stored and lower

bits that indicate a position of processing target
instruction that is included in the processing packet,
the linker comprising:
relocation information detecting means for detecting
a label in the relocatable code that should be resolved by
a difference in addresses between two specified
instructions, and obtaining the addresses of the two
specified instructions;

program counter relative value calculating means for
calculating a program counter relative value by subtracting
an address of one of the two specified instructions from an
address of another of the two specified instructions; and
replacing means for replacing the label with the
program counter relative value calculated by the program
counter relative value calculating means.

21. The linker of Claim 20,

wherein the program counter relative value
calculating means includes a lower bit subtracting unit and
an upper bit subtracting unit,

the lower bit subtracting unit subtracting lower bits
of the address of the one of the two specified instructions
from lower bits of the address of the other of the two
specified instructions, for setting a result of a
subtraction as lower bits of the program counter relative
value, and sending any carry generated in the subtraction
to the upper bit subtracting unit, and

12 the upper bit subtracting unit subtracting upper bits
13 of the address of one of the two specified instructions and
14 any carry received from the lower bit subtracting unit from
15 upper bits of the address of the other of the two specified
16 instructions, and for setting a result of a subtraction as
17 upper bits of the program counter relative value.

1 22. The linker of Claim 20,

2 wherein the program counter relative value
3 calculating means includes a lower bit subtracting unit and
4 an upper bit subtracting unit,

5 the lower bit subtracting unit subtracting lower bits
6 of the address of one of the two specified instructions
7 from lower bits of the address of the other of the two
8 specified instructions without generating a carry and
9 setting a result of a subtraction as lower bits of the
10 program counter relative value, and

11 the upper bit subtracting unit subtracting upper bits
12 of the address of one of the two specified instructions
13 from upper bits of the address of the other of the two
14 specified instructions, and for setting a result of a
15 subtraction as upper bits of the program counter relative
16 value.

1 23. The linker of Claim 20,

2 wherein the program counter relative value
3 calculating means subtracts upper bits of an address of one

4 of the two specified instructions from upper bits of an
5 address of the other of the two specified instructions,
6 sets a result of a subtraction as upper bits of the program
7 counter relative value, and sets lower bits of the other of
8 the two specified instructions as lower bits of the program
9 counter relative value.

1 24. A disassembler that receives an indication of an
2 address of an instruction in object code and outputs an
3 assembler name of the instruction at the indicated address,
4 each address of an instruction in the object code having
5 upper bits that indicate a memory address at which a
6 processing packet is stored and lower bits that indicate a
7 position of processing target instruction that is included
8 in the processing packet,

9 the disassembler comprising:

10 program counter relative value extracting means for
11 extracting, when the indicated instruction includes a
12 program counter relative value, the program counter
13 relative value from the indicated instruction;

14 label addressing calculating means for adding an
15 address of the indicated instruction to the extracted
16 program counter relative value and setting an addition
17 result as a label address;

18 storing means for storing a label name corresponding
19 to each label address; and

20 searching means for searching the storing means for a

21 label name that corresponds to the calculated label address
22 and outputting the corresponding label name.

1 25. The disassembler of Claim 24,

2 wherein the label address calculating means includes
3 a lower bit calculating unit and an upper bit calculating
4 unit,

5 the lower bit calculating unit for adding lower bits
6 of the address of the indicated instruction and lower bits
7 of the program counter relative value, setting a result of
8 an addition as lower bits of a label address, and sending
9 any carry generated by the addition to the upper bit
10 calculating unit, and

11 the upper bit calculating unit adding upper bits of
12 the address of the indicated instruction, upper bits of the
13 program counter relative value, and any carry received from
14 the lower bit calculating unit, and setting a result of the
15 an addition as upper bits of the label address.

1 26. The disassembler of Claim 24,

2 wherein the label address calculating means includes
3 a lower bit calculating unit and an upper bit calculating
4 unit,

5 the lower bit calculating unit adding lower bits of
6 the address of the indicated instruction and lower bits of
7 the program counter relative value without generating a
8 carry, and setting a result of an addition as lower bits of

9 a label address, and

10 the upper bit calculating unit adding upper bits of
11 the address of the indicated instruction and upper bits of
12 the program counter relative value, and setting a result of
13 an addition as upper bits of the label address.

1 27. The disassembler of Claim 24, wherein

2 the label address calculating means adds upper bits
3 of the address of the indicated instruction and upper bits
4 of the program counter relative value, sets a result of an
5 addition as upper bits of the label address, and sets lower
6 bits of the program counter relative value as lower bits of
the label address.

7 28. A debugger that receives an indication of an address of
8 an instruction in object code and replaces the instruction
9 at the indicated address with a replacement instruction,
10 each address of an instruction in the object code having
11 upper bits that indicate a memory address at which a
12 processing packet is stored and lower bits that indicate a
13 position of processing target instruction that is included
in the processing packet,

the debugger comprising:

14 processing packet reading means for reading a
15 processing packet that is indicated by upper bits of the
16 indicated address from the memory and writing the
17 processing packet into an instruction buffer;

instruction writing means for writing the replacement instruction into the processing packet in the instruction buffer over an instruction that is indicated by the lower bits of the indicated address; and

processing packet writing means for writing the processing packet in the instruction buffer back into the memory after the replacement instruction has been written.

1 29. A compiler that generates an instruction sequence from
2 source code,

3 the compiler generating a program counter relative
4 value calculating instruction that is executed by a
5 processor, the program counter relative value calculating
6 instruction being an instruction that performs a
7 calculation using a first value and a program counter
8 relative value and uses a result of the calculation to
9 update the first value, the first value being one of

10 (a) a value of a program counter stored in a
11 register, and

12 (b) the value stored in a program counter of the
13 processor,

14 wherein upper bits of the first value indicate a
15 memory address at which a processing packet is stored, and
16 lower bits of the first value of the program counter
17 indicate a processing target instruction that is included
18 in the processing packet.

1 30. The compiler of Claim 29,
2 wherein the processor includes a lower bit
3 calculating unit and an upper bit calculating unit,
4 the program counter relative value calculating
5 instruction having the lower bit calculating unit perform a
6 lower bit calculation and the upper bit calculating unit
7 perform an upper bit calculation,
8 the lower bit calculation being an addition using
9 lower bits of the first value and lower bits of the value
10 of the program counter relative value, where a result of
11 the lower bit calculation is set as the lower bits of the
12 first value and any generated carry is sent to the upper
13 bit calculating unit, and
14 the upper bit calculation being an addition using
15 upper bits of the first value, upper bits of the value of
16 the program counter relative value and any carry received
17 from the lower bit calculating unit, where a result of the
18 upper bit calculation is set as the upper bits of the first
19 value.

1 31. The compiler of Claim 29,
2 wherein the processor includes a lower bit
3 calculating unit and an upper bit calculating unit,
4 the program counter relative value calculating
5 instruction having the lower bit calculating unit perform a
6 lower bit calculation and the upper bit calculating unit
7 perform an upper bit calculation,

8 the lower bit calculation being an addition using
9 lower bits of the first value and lower bits of the value
10 of the program counter relative value that does not
11 generate a carry, where a result of the lower bit
12 calculation is set as the lower bits of the first value,
13 and

14 the upper bit calculation being a calculation using
15 upper bits of the first value and upper bits of the value
16 of the program counter relative value, where a result of
17 the upper bit calculation is set as the upper bits of the
18 first value.

19
20
21 32. The compiler of Claim 29,

22 wherein the processor includes an upper bit
23 calculating unit,

24 the program counter relative value calculating
25 instruction having the upper bit calculating unit perform
26 an upper bit calculation and setting lower bits of the
27 program counter relative value as lower bits of the first
28 value, and

29 the upper bit calculation being an addition using
30 upper bits of the first value and upper bits of the value
31 of the program counter relative value, where a result of
32 the upper bit calculation is set as the upper bits of the
33 first value.

34
35 33. A computer-readable recording medium storing an

instruction sequence optimizing program that generates optimized code from an instruction sequence, the instruction sequence optimizing program including:

- an address assigning step for estimating a size of each instruction in the instruction sequence and assigning an address to each instruction, upper bits of each address indicating a memory address at which a processing packet is stored and lower bits of each address indicating a processing target instruction in the processing packet;
- a label detecting step (1) for detecting a label, which should be resolved by an address of a specified instruction, from the instruction sequence, and obtaining the address of the specified instruction, and
 - (2) for detecting a label, which should be resolved by a difference in addresses of two specified instructions, from the instruction sequence, and obtaining the addresses of the two specified instructions;
- a program counter relative value calculating step for calculating, when a label which should be resolved by a difference in addresses of two specified instructions has been detected, a program counter relative value by subtracting an address of one of the two specified instructions from an address of another of the two specified instructions;
- a converting step
 - (1) for converting an instruction that has a label

that should be resolved by an address of a specified instruction into an instruction with a size that is based on a size of the address of the specified instruction,

(2) for converting an instruction that has a label that should be resolved by a difference in addresses of two specified instructions into an instruction with a size that is based on a size of the program counter relative value calculated from the addresses of the two specified instructions; and

an optimized code generating step for generating optimized code by converting addresses of instructions in accordance with the sizes of instructions after conversion in the converting step.

34. The computer-readable recording medium of Claim 33, wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower bits of the address of the one of the two specified instructions from lower bits of the address of the other of the two specified instructions, for setting a result of a subtraction as lower bits of the program counter relative value, and sending any carry generated in the subtraction to the upper bit subtracting substep, and

the upper bit subtracting substep subtracting upper

bits of the address of one of the two specified instructions and any carry received from the lower bit subtracting substep from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

35. The computer-readable recording medium of Claim 33, wherein the program counter relative value calculating step includes a lower bit subtracting substep and an upper bit subtracting substep, the lower bit subtracting substep subtracting lower bits of the address of one of the two specified instructions from lower bits of the address of the other of the two specified instructions without generating a carry and setting a result of a subtraction as lower bits of the program counter relative value, and

the upper bit subtracting substep subtracting upper bits of the address of one of the two specified instructions from upper bits of the address of the other of the two specified instructions, and for setting a result of a subtraction as upper bits of the program counter relative value.

36. The computer-readable recording medium of Claim 33, wherein the program counter relative value calculating step subtracts upper bits of an address of one

4 of the two specified instructions from upper bits of an
5 address of the other of the two specified instructions,
6 sets a result of a subtraction as upper bits of the program
7 counter relative value, and sets lower bits of the other of
8 the two specified instructions as lower bits of the program
9 counter relative value.

1 37. A computer-readable recording medium storing an
2 assembler program that generates relocatable code from
3 optimized code that have been generated from an instruction
4 sequence, each address of an instruction in the optimized
5 code having upper bits that indicate a memory address at
6 which a processing packet is stored and lower bits that
7 indicate a position of processing target instruction that
8 is included in the processing packet,

9 the assembler program comprising:

10 a label detecting step for detecting a label in the
11 instruction sequence that should be resolved by a
12 difference in addresses between two specified instructions,
13 and obtaining the addresses of the two specified
14 instructions;

15 a program counter relative value calculating step for
16 calculating a program counter relative value by subtracting
17 an address of one of the two specified instructions from an
18 address of another of the two specified instructions; and

19 a replacing step for replacing the label with the
20 program counter relative value calculated by the program

21 counter relative value calculating step.

1 38. The computer-readable recording medium of Claim 37,
2 wherein the program counter relative value
3 calculating step includes a lower bit subtracting substep
4 and an upper bit subtracting substep,
5 the lower bit subtracting substep subtracting lower
6 bits of the address of the one of the two specified
7 instructions from lower bits of the address of the other of
8 the two specified instructions, for setting a result of a
9 subtraction as lower bits of the program counter relative
10 value, and sending any carry generated in the subtraction
11 to the upper bit subtracting substep, and

12 the upper bit subtracting substep subtracting upper
13 bits of the address of one of the two specified
14 instructions and any carry received from the lower bit
15 subtracting substep from upper bits of the address of the
16 other of the two specified instructions, and for setting a
17 result of a subtraction as upper bits of the program
18 counter relative value.

1 39. The computer-readable recording medium of Claim 37,
2 wherein the program counter relative value
3 calculating step includes a lower bit subtracting substep
4 and an upper bit subtracting substep,
5 the lower bit subtracting substep subtracting lower
6 bits of the address of one of the two specified

7 instructions from lower bits of the address of the other of
8 the two specified instructions without generating a carry
9 and setting a result of a subtraction as lower bits of the
10 program counter relative value, and

11 the upper bit subtracting substep subtracting upper
12 bits of the address of one of the two specified
13 instructions from upper bits of the address of the other of
14 the two specified instructions, and for setting a result of
15 a subtraction as upper bits of the program counter relative
16 value.

40. The computer-readable recording medium of Claim 37,
wherein the program counter relative value
calculating step subtracts upper bits of an address of one
of the two specified instructions from upper bits of an
address of the other of the two specified instructions,
sets a result of a subtraction as upper bits of the program
counter relative value, and sets lower bits of the other of
the two specified instructions as lower bits of the program
counter relative value.

41. A computer-readable recording medium storing a linker
program that generates object code from relocatable code
that has been generated from an instruction sequence, each
address of an instruction in the optimized code having
upper bits that indicate a memory address at which a
processing packet is stored and lower bits that indicate a

position of processing target instruction that is included
in the processing packet,

the linker program comprising:

a relocation information detecting step for detecting
a label in the relocatable code that should be resolved by
a difference in addresses between two specified
instructions, and obtaining the addresses of the two
specified instructions;

a program counter relative value calculating step for
calculating a program counter relative value by subtracting
an address of one of the two specified instructions from an
address of another of the two specified instructions; and

a replacing step for replacing the label with the
program counter relative value calculated by the program
counter relative value calculating step.

42. The computer-readable recording medium of Claim 41,

wherein the program counter relative value
calculating step includes a lower bit subtracting substep
and an upper bit subtracting substep,

the lower bit subtracting substep subtracting lower
bits of the address of the one of the two specified
instructions from lower bits of the address of the other of
the two specified instructions, for setting a result of a
subtraction as lower bits of the program counter relative
value, and sending any carry generated in the subtraction
to the upper bit subtracting substep, and

12 the upper bit subtracting substep subtracting upper
13 bits of the address of one of the two specified
14 instructions and any carry received from the lower bit
15 subtracting substep from upper bits of the address of the
16 other of the two specified instructions, and for setting a
17 result of a subtraction as upper bits of the program
18 counter relative value.

1 43. The computer-readable recording medium of Claim 41,
2 wherein the program counter relative value
3 calculating step includes a lower bit subtracting substep
4 and an upper bit subtracting substep,
5 the lower bit subtracting substep subtracting lower
6 bits of the address of one of the two specified
7 instructions from lower bits of the address of the other of
8 the two specified instructions without generating a carry
9 and setting a result of a subtraction as lower bits of the
10 program counter relative value, and
11 the upper bit subtracting substep subtracting upper
12 bits of the address of one of the two specified
13 instructions from upper bits of the address of the other of
14 the two specified instructions, and for setting a result of
15 a subtraction as upper bits of the program counter relative
16 value.

1 44. The computer-readable recording medium of Claim 41,
2 wherein the program counter relative value

calculating step subtracts upper bits of an address of one of the two specified instructions from upper bits of an address of the other of the two specified instructions, sets a result of a subtraction as upper bits of the program counter relative value, and sets lower bits of the other of the two specified instructions as lower bits of the program counter relative value.

45. A computer-readable recording medium storing a compiler program that generates an instruction sequence from source code,

the compiler program generating a program counter relative value calculating instruction that is executed by a processor, the program counter relative value calculating instruction being an instruction that performs a calculation using a first value and a program counter relative value and uses a result of the calculation to update the first value, the first value being one of

(a) a value of a program counter stored in a register, and

(b) the value stored in a program counter of the processor,

wherein upper bits of the first value indicate a memory address at which a processing packet is stored, and lower bits of the first value of the program counter indicate a processing target instruction that is included in the processing packet.

1 46. The computer-readable recording medium of Claim 45,
2 wherein the processor includes a lower bit
3 calculating unit and an upper bit calculating unit,
4 the program counter relative value calculating
5 instruction having the lower bit calculating unit perform a
6 lower bit calculation and the upper bit calculating unit
7 perform an upper bit calculation,
8 the lower bit calculation being an addition using
9 lower bits of the first value and lower bits of the value
10 of the program counter relative value, where a result of
11 the lower bit calculation is set as the lower bits of the
12 first value and any generated carry is sent to the upper
13 bit calculating unit, and
14 the upper bit calculation being an addition using
15 upper bits of the first value, upper bits of the value of
16 the program counter relative value and any carry received
17 from the lower bit calculating unit, where a result of the
18 upper bit calculation is set as the upper bits of the first
19 value.

1 47. The computer-readable recording medium of Claim 45,
2 wherein the processor includes a lower bit
3 calculating unit and an upper bit calculating unit,
4 the program counter relative value calculating
5 instruction having the lower bit calculating unit perform a
6 lower bit calculation and the upper bit calculating unit

perform an upper bit calculation,

the lower bit calculation being an addition using lower bits of the first value and lower bits of the value of the program counter relative value that does not generate a carry, where a result of the lower bit calculation is set as the lower bits of the first value, and

the upper bit calculation being a calculation using upper bits of the first value and upper bits of the value of the program counter relative value, where a result of the upper bit calculation is set as the upper bits of the first value.

48. The computer-readable recording medium of Claim 45, wherein the processor includes an upper bit calculating unit,

the program counter relative value calculating instruction having the upper bit calculating unit perform an upper bit calculation and setting lower bits of the program counter relative value as lower bits of the first value, and

the upper bit calculation being an addition using upper bits of the first value and upper bits of the value of the program counter relative value, where a result of the upper bit calculation is set as the upper bits of the first value.